In the Claims

Please amend the claims as follows:

1. (Previously Amended) A method for emulation communications via a test data input port and boundary-scan architecture providing serial access to a serial connection of a plurality of registers disposed in a plurality of modules, each of the plurality of modules including at least one of the plurality of registers, comprising the steps of:

selecting for communication one of said plurality of modules, nonselected modules being nonresponsive to data on said serial connection;

supplying to the test data input port for communication to the boundary-scan architecture a serial signal having a first logic state for a number of cycles greater in number than a number of bits of the serial connection of the plurality of registers;

following supply of said serial signal, supplying to the test data input port for communication to the boundary-scan architecture a start bit having a second logic state opposite to said first logic state followed by a predetermined number of data bits;

at said selected module detecting said start bit within the boundary-scan architecture and storing said predetermined number of data bits.

2. (Original) The method of claim 1, wherein:

said step of storing said predetermined number of data bits consists of storing said predetermined number of data bits in a program visible data register.

3. (Original) The method of claim 1, further comprising:

at said selected module, interpreting said predetermined number of data bits as an instruction and performing a function corresponding to said instruction.

4. (Previously Amended) The method of claim 1, wherein the boundary-scan architecture includes a test data output port following a last of the serial connection of registers, the method further comprising:

at said selected module, supplying a serial signal having said first logic state to following registers in the serial connection of the plurality of registers for a predetermined number of cycles and supplying to following registers in the serial connection of the plurality of registers a start bit having a second logic state opposite to said first logic state followed by said predetermined number of data bits.